WHAT IS CLAIMED IS:

1. A method for fabricating an integrated circuit, said method comprising the steps of:

forming a first dielectric layer;

forming a second dielectric layer above the first dielectric layer, the second dielectric layer being capable of being selectively etched with respect to the first dielectric layer;

etching holes and/or trenches in the first and second dielectric layers;

filling the holes and/or trenches with metal in order to form electrical connection elements;

forming at least a third dielectric layer; and

selectively etching holes and/or trenches in the third dielectric layer and the second dielectric layer with respect to the first dielectric layer and the elements, in order to control the depth of the etch.

2. The method as defined in claim 1, further comprising the step of forming a fourth dielectric layer above the third dielectric layer, the fourth dielectric layer being capable of being selectively etched with respect to the third dielectric layer.

3. The method as defined in claim 2, further comprising the steps of:

etching the third and fourth dielectric layers;

selectively etching the third dielectric layer with respect to the second dielectric layer; and

selectively etching the second dielectric layer with respect to the first dielectric layer.

4. The method as defined in claim 1, further comprising the step of forming an additional dielectric layer on the second dielectric layer.

5. The method as defined in claim 4, further comprising the steps of:

selectively etching the third dielectric layer and the additional dielectric layer with respect to the second dielectric layer; and

filling resulting holes with metal in order to form electrical connection elements.

6. The method as defined in claim 1, further comprising the step of repeating the previous steps in order to form lines and vias of a subsequent metallization level.

7. The method as defined in claim 1, further comprising the step of repeating the previous steps at least two times in order to form lines and vias of at least two subsequent metallization levels.

8. A machine-readable medium encoded with a program for controlling at least one manufacturing machine in order to fabricate an integrated circuit, said program containing instructions for performing the steps of:

forming a first dielectric layer;

forming a second dielectric layer above the first dielectric layer, the second dielectric layer being capable of being selectively etched with respect to the first dielectric layer;

etching holes and/or trenches in the first and second dielectric layers;

filling the holes and/or trenches with metal in order to form electrical connection elements;

forming at least a third dielectric layer; and

selectively etching holes and/or trenches in the third dielectric layer and the second dielectric layer with respect to the first dielectric layer and the elements, in order to control the depth of the etch.

9. The machine-readable medium as defined in claim 8, wherein said program further contains instructions for performing the step of forming a fourth dielectric layer above the third dielectric layer, the fourth dielectric layer being capable of being selectively etched with respect to the third dielectric layer.

10. The machine-readable medium as defined in claim 9, wherein said program further contains instructions for performing the steps of:

etching the third and fourth dielectric layers;

selectively etching the third dielectric layer with respect to the second dielectric layer; and

selectively etching the second dielectric layer with respect to the first dielectric layer.

11. The machine-readable medium as defined in claim 8, wherein said program further contains instructions for performing the step of forming an additional dielectric layer on the second dielectric layer.

12. The machine-readable medium as defined in claim 11, wherein said program further contains instructions for performing the steps of:

selectively etching the third dielectric layer and the additional dielectric layer with respect to the second dielectric layer; and

filling resulting holes with metal in order to form electrical connection elements.

13. The machine-readable medium as defined in claim 8, wherein said program further contains instructions for performing the step of repeating the previous steps in order to form lines and vias of a subsequent metallization level.

14. The machine-readable medium as defined in claim 8, wherein said program further contains instructions for performing the step of repeating the previous steps at least two times in order to form lines and vias of at least two subsequent metallization levels.

15. An integrated circuit of the type having metallization levels separated by dielectric layers and metallized vias connecting lines of different metallization levels, said integrated circuit comprising:

at least first and second metallization levels;

at least first and second superposed dielectric layers located above the first metallization level;

a third dielectric layer located above the first and second dielectric layers; and

at least one electrical connection element provided in the third dielectric layer and passing through the second dielectric layer until it comes into contact with the first dielectric layer.

16. The integrated circuit as defined in claim 15, further comprising at least one metallized via having an upper surface that is flush with an upper surface of the second dielectric layer.

17. The integrated circuit as defined in claim 16,

wherein the metallized via has a lateral surface adjacent to its upper surface, and

the electrical connection element includes one portion that is in contact with the upper surface of the metallized via and another portion at the level of the second dielectric layer that is in contact with the lateral surface of the metallized via.

18. The integrated circuit as defined in claim 15, further comprising:

a third metallization level;

at least fourth and fifth superposed dielectric layers located above the second metallization level;

a sixth dielectric layer located above the fourth and fifth dielectric layers; and

at least one additional electrical connection element provided in the sixth dielectric layer and passing through the fifth dielectric layer until it comes into contact with the fourth dielectric layer.

19. The integrated circuit as defined in claim 18, further comprising:

at least one additional metallized via having an upper surface that is flush with an upper surface of the second dielectric layer,

wherein the metallized via has a lateral surface adjacent to its upper surface, and

the electrical connection element includes one portion that is in contact with the upper surface of the metallized via and another portion at the level of the second dielectric layer that is in contact with the lateral surface of the metallized via.